REMARKS/ARGUMENTS

The claims are 2-6 and 9-12. Claims 1, 7 and 8 have been canceled in favor of new claim 12 to more particularly define the invention. Accordingly, claims 1, 7 and 8 have been canceled and claims 2, 5, 6, 9 and 11 have been amended to depend on new claim 12. These claims and the remaining claims have also been amended to improve their form. Support may be found, *inter alia*, in the paragraph bridging pages 7 and 8, in the first full paragraph on page 12, and in FIG. 2d. Reconsideration is expressly requested.

Claims 1-11 were objected to as using structural language instead of method language. Claims 1-11 were also rejected under 35 U.S.C. 112, second paragraph, as being indefinite as lacking antecedent basis for the limitation "the intermediate layer" in step d, lines 2-3, of claim 1. In response, Applicant has canceled claims 1, 7 and 8 in favor of new claim 12, and has amended the remaining claims to improve their form. It is respectfully submitted that the currently pending claims fully comply with 35 U.S.C. §112, second paragraph, and Applicant respectfully requests that the Examiner's objection to the claims on the basis of these informalities be withdrawn.

Claims 1-2 and 5-10 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Ishii et al. U.S. Patent No. 5,919,713*. The remaining claims 3, 4 and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Ishii et al.* in view of *Nakanishi et al. U.S. Published Patent Application 2001/0005043* (claim 3), *Sugino et al. U.S. Published Patent Application 2002/0055238* (claim 4), or *Mignardi et al. U.S. Patent No. 5,597,767* (claim 11). Essentially, the Examiner's position was that *Ishii et al.* discloses the method recited in the claims except for an adhesive material having a lower adhesion to the front face surface of the wafer when a higher temperature is used, which is said to be shown by *Nakanishi et al.*, except for performing the individual release of the semiconductors circuits from the carrier mechanically to overcome the adhesion force of the attachment material to the front face of the wafer, which is said to be shown by *Sugino et al.*, and except for performing an electrical function test of the semiconductor circuits after separation, which is said to be shown by *Mignardi et al.*

This rejection is expressly traversed.

As set forth in new claim 12, Applicant's invention provides a method for producing individual monolithically integrated

semiconductor circuit arrangements from a wafer composite substrate. In accordance with Applicant's method, a plurality of separate component structures are formed that include monolithic semiconductor circuits and conductive surfaces on a front face surface of a wafer. The front face surface of the wafer is covered with a protective layer to form a wafer composite substrate. The wafer is attached to a support via an attachment layer applied over the support. The substrate is reduced to a selected thickness. Passage holes are produced through the substrate up to the conductive surfaces on the front face surface. Separating trenches are produced between the monolithic semiconductor circuits up to or into the attachment layer. This step includes removal of the protective layer under the separating trenches and lateral under-etching of the substrate. A back face metallization is deposited on a back face of the substrate and electrical connections are formed through the passage holes, and the semiconductor circuits are individually released from the support for further individual processing.

With these method steps, the secure and stable handling of the wafer is made possible, particularly in the case where the substrate has a low thickness. By removal of the protective layer under the separating trenches and lateral under-etching of

the substrate during production of the separating trenches between the monolithic semiconductor circuits, it is possible to deposit the metal from the back face metallization and the interfacial connection after completion of the separating trenches, over the entire area, without any metallization bridge being formed over the separating trenches.

Moreover, as more specifically recited in claim 3, as amended, an adhesive material is used for the attachment layer wherein the adhesive material has a lower adhesion to the front face surface of the wafer at a higher temperature. The use of an adhesive that can be dissolved with heat facilitates the individual release of the mechanically separated ICs from the chips. In addition, as more specifically recited in claim 11, as amended, Applicant's invention provides a method in which an electrical function test of the semiconductor circuits is performed after separation.

None of the cited references discloses or suggests a method of producing individual monolithically integrated semiconductor circuit arrangements from a wafer composite substrate having the specific process steps recited in new claim 12 or teaches the benefit of producing separating trenches between the monolithic

semiconductor circuits up to or into the attachment layer, including removal of the protective layer under the separating trenches and lateral under-etching of the substrate.

Ishii et al. discloses a method for fabricating a semiconductor device in which the separating trenches are brought up to the attachment layer, but not into the attachment layer. The trenches go up to the attachment layer only where no passivation layer is present. Contrary to the Examiner's position that under-etching of the protective layer occurs because of the isotropic behavior of a wet etching process, it is respectfully submitted that etching **into** an attachment layer or under-etching of the protective layer fails to take place in *Ishii*.

In the paragraph cited by the Examiner, in column 6, lines 11-23 of *Ishii et al.*, it is explicitly stated that the substrate 1 is exposed to the wet etching process, that the dicing region 11 is selectively etched as shown in FIG. 2C, and that the rigid connection part 16 is not affected by the etching; however, according to column 5, lines 20 and 21 of *Ishii et al.*, these connection parts are part of the passivation film, which corresponds to protective layer 23 shown in Applicant's FIG. 1.

Ishii et al. therefore explicitly states that the material of the protective layer is **not** attacked by the etching solution during the etching of the trenches. There is also no indication of any kind that can be derived from *Ishii et al.* to show that etching is supposed to reach into the attachment layer 18 in *Ishii et al.* According to col. 6, line 46, of *Ishii et al.*, the attachment layer 18 is dissolved by means of an organic solvent, while an acid is used for etching the trenches, according to line 16, column 6 of *Ishii et al.*

In contrast to *Ishii et al.*, in Applicant's invention as set forth in claim 12 under-etching of the protective layer takes place. As a result, during the metal coating of the back (see transition from FIG. 2d to FIG. 2e), no metallic connection between adjacent chips occurs at the trenches. In *Ishii et al.*, however, such a connection of the metallic layer 21 occurs according to FIG. 2D of *Ishii et al.*, and it must be removed again by means of special lithographic exposure and anisotropic etching processes.

Moreover, it is respectfully submitted that contrary to the Examiner's position, the chips are not individually taken off the

rigid carrier in *Ishii et al.* Instead, in *Ishii et al.*, a mechanical connection of the chips is explicitly intended by means of the rigid bridges 16, and the mechanically connected chips are all released from the rigid carrier 19 together, at the transition from FIG. 2D to FIG. 2E of *Ishii et al.*, and attached on a flexible band 23 (see FIG. 2E or FIG. 5B of *Ishii et al.*). In this connection, the individual chips are still mechanically connected by way of the bridges 16. Separation of the chips can take place in that the flexible band 23 is stretched in the longitudinal direction, thereby causing the rigid bridges 16 to tear off.

Accordingly, it is respectfully submitted that the Examiner's assertion that in *Ishii et al.*, the chips are "individually released from the rigid carrier," is incorrect. Instead, col. 6, line 48 of *Ishii et al.* ("while maintaining alignment of the semiconductor chips") makes it clear that the chips are released from the rigid carrier together, in a state in which they are connected with one another.

The defects and deficiencies of the primary reference to *Ishii et al.* are nowhere remedied by the secondary references to *Nakanishi, Sugino et al., or Mignardi et al.* *Nakanishi* which has been cited with respect to claim 3, discloses a technique which performs the thinning of a wafer and the separation thereof from a support

substrate. Although the Examiner has taken the position that FIGS. 1A-1C of *Nakanishi* discloses adhesive layers 33 and 36 for bonding a semiconductor wafer and support substrates, it is respectfully submitted that only the layer 36 serves to connect the semiconductor chip with a carrier. The layer 33 is a connection between two carriers. Therefore, only the layer 36 is comparable with the attachment layer as recited in claim 3, as amended; however, according to column 7, paragraph 0101 of *Nakanishi et al.*, layer 36 is dissolved not with heat, but rather under the effect of a solvent, for example isopropyl alcohol. *Nakanishi et al.* therefore fails to disclose or suggest the attachment of chips by means of an adhesive that can be dissolved with heat, but rather explicitly teaches attaching the chips on a carrier using a material that is removed by a solvent.

In contrast Applicant's method as recited in claim 3 uses an adhesive that can be dissolved by means of the effect of heat, which is particularly advantageous in connection with the release of individual chips. In contrast to dissolving the attachment layer by means of a solvent, with Applicant's method it is not the entire layer that is removed for all the chips, but instead the holding force is merely reduced by means of heating the attachment layer, and the individual chip can be lifted off the attachment layer with reduced force.

Sugino et al., which has been cited with respect to claim 4, discloses a process for producing a semiconductor device in which an adhesive layer 32 together with the chips 3 is detachable from the base 31 of a dicing/die bond sheet 30. When the chips 3 are picked up, the adhesive layer 32 remains adhering to the back of the chips 3 and is detached from the base 31. However, there is no disclosure or suggestion in *Sugino et al.* of a process as recited in new claim 12 in which separating trenches are produced between the monolithic semiconductor circuits up to or into the attachment layer, including removal of the protective layer under the separating trenches and lateral under-etching of the substrate.

Mignardi et al., which has been cited with respect to claim 11, discloses a method of separating wafers, such as those used for semiconductor device manufacture, into die. Although the Examiner has taken the position that *Mignardi et al.* makes it obvious to undertake a function test after separation of the individual chips, it is respectfully submitted that *Mignardi et al.* explicitly states the opposite. Specifically, in column 4, lines 26 to 39 of *Mignardi et al.*, it is explicitly stated that the function test is carried out in step 15. In Fig. 1 to Fig. 3 of *Mignardi et al.*, it is unambiguously evident that the separation of individual chips takes place in step 17, after step 15, i.e. that the test takes place before separation. In Fig. 2 of *Mignardi et al.*, step 15 is shown in even greater detail,

and contains a step 24 as a test. Therefore, it is respectfully submitted that *Mignardi et al.* fails to disclose or suggest performing an electrical function test of the semiconductor circuits after separation as recited in Applicant's claim 11, as amended.

Accordingly, it is respectfully submitted that new claim 12 and dependent claims 2-6 and 9-11 are patentable over the cited references.

In summary, claims 2-6 and 9-11 have been amended, claims 1 and 7-8 have been canceled, and new claim 12 has been added. In view of the foregoing, it is respectfully requested that the claims be allowed and that this case be passed to issue.

Respectfully submitted,
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I hereby certify that this correspondence is being sent by facsimile-transmission to the Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 7, 2006.

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